

PATENT

This listing of claims will replace all prior versions and listings of the claims in this application:

Claim 1 (original) A computing system comprising:

a general purpose microprocessor for executing a predetermined software application; and,

a monitoring microprocessor having an assurance characteristic which is higher and having a performance characteristic which is lower than that of said general purpose microprocessor; said monitoring microprocessor coupled to and monitoring said general purpose microprocessor, where said monitoring does not involve real-time comparison of parallel computations made on parallel microprocessors.

Claim 2 (original) A system of claim 1 wherein said general purpose microprocessor generates state transitions as said predetermined software application is executed.

Claim 3 (original) A system of claim 2 wherein said monitoring microprocessor monitors said state transitions and generates a fault signal when a determination of invalidity of said state transitions is made by said monitoring microprocessor.

Claim 4 (original) A system of claim 3 wherein said fault signal is a reset signal sent to said general purpose microprocessor.

Claim 5 (currently amended) A computing system of claim 4 comprising:

PATENT

a general purpose microprocessor for executing a predetermined software application;

a monitoring microprocessor having an assurance characteristic which is higher and having a performance characteristic which is lower than that of said general purpose microprocessor, said monitoring microprocessor coupled to and monitoring said general purpose microprocessor, where said monitoring does not involve real-time comparison of parallel computations made on parallel microprocessors;

wherein said general purpose microprocessor generates state transitions as said predetermined software application is executed;

wherein said monitoring microprocessor monitors said state transitions and generates a fault signal when a determination of invalidity of said state transitions is made by said monitoring microprocessor;

wherein said fault signal is a reset signal sent to said general purpose microprocessor; and

wherein said monitoring microprocessor has associated therewith a certification from an agency of the US government which regulates safety.

Claim 6 (original) A system of claim 5 wherein said predetermined software application has associated therewith a certification from an agency of the U.S. government which regulates safety.

PATENT

Claim 7 (original) A system of claim 1 wherein said monitoring involves comparing a value generated by said general purpose microprocessor with a value based upon predetermined criteria, which relate to physical and operational limitations of an aircraft.

Claim 8 (original) A system of claim 7 wherein said predetermined criteria include limitations on rates of change of said value generated by said general purpose microprocessor.

Claim 9 (original) A system of claim 7 wherein said predetermined criteria are stored in a look-up table coupled to said monitoring microprocessor.

Claim 10 (previously amended) A computing system comprising:

a general purpose microprocessor for executing a predetermined software application;

a monitoring microprocessor having an assurance characteristic which is higher and having a performance characteristic which is lower than that of said general purpose microprocessor; said monitoring microprocessor coupled to and monitoring said general purpose microprocessor, where said monitoring does not involve real-time comparison of parallel computations made on parallel microprocessors;

wherein said monitoring involves comparing a value generated by said general purpose microprocessor with a value based upon predetermined criteria, which relate to physical and operational limitations of an aircraft; and

PATENT

wherein said general purpose microprocessor is coupled with an instruction trace buffer disposed on a chip carrying said general purpose microprocessor, wherein said instruction trace buffer temporarily stores instructions as they are executed by said general purpose microprocessor, so as to be retrievable in an event that a fault signal is generated by said monitoring microprocessor.

Claim 11 (previously amended) A computing system comprising:

a general purpose microprocessor for executing a predetermined software application;

a monitoring microprocessor having an assurance characteristic which is higher and having a performance characteristic which is lower than that of said general purpose microprocessor; said monitoring microprocessor coupled to and monitoring said general purpose microprocessor, where said monitoring does not involve real-time comparison of parallel computations made on parallel microprocessors; and

wherein said monitoring microprocessor and said general purpose microprocessor execute derived dissimilar programs, which are derived from a common predetermined software application, where a software conversion tool is used to derive said dissimilar programs.

Claim 12 (original) A system of claim 11 wherein said software conversion tool is a tool having associated therewith a certification from an agency of the US government which regulates safety.

PATENT

Claim 13 (original) A system of claim 12 wherein software conversion tool causes said predetermined software application to generate state transition signals when executed on said general purpose microprocessor.

Claim 14 (previously amended) An avionics system comprising:

disposed on-board an aircraft, means for executing a predetermined avionics software application which has been certified by an agency of the U.S. government which regulates safety;

disposed on-board an aircraft, means for enhancing an integrity characteristic of said means for executing; and,

said means for enhancing not involving a comparison of outputs of parallel computing machines.

Claim 15 (original) An avionics system of claim 14 wherein said means, on-board an aircraft, for enhancing is a virtual machine implemented with said means, on-board an aircraft, for executing.

Claim 16 (original) An avionics system of claim 14 wherein said means, on-board an aircraft, for enhancing is an independent microprocessor.

Claim 17 (original) An avionics system of claim 14 wherein said means, on-board an aircraft, for enhancing, comprises:

PATENT

a comparison between 1) a value generated by said means, on-board an aircraft, for executing; and 2) a predetermined criteria indicating a validity characteristic of said value.

Claim 18 (previously amended) A method of enhancing an integrity characteristic of an airborne avionics computing system comprising the steps of:

providing a first microprocessor, which executes a predetermined avionics software application, and thereby generates a calculated value;

providing a second microprocessor which is coupled to said first microprocessor; and,

enhancing an integrity of said calculated value by monitoring, with said second processor, an output of said first microprocessor, where said monitoring is not a comparison of parallel computations made by parallel processors, and said output is not a failure status of said first microprocessor.

Claim 19 (original) A method of claim 18 wherein said step of enhancing includes the steps of:

generating state transition signals during an execution of said predetermined avionics software application;

comparing said state transition signals, by said second microprocessor, against predetermined criteria and generating a fault signal in response thereto; and,

PATENT

resetting said first microprocessor in response to said fault signal.

Claim 20 (original) A method of claim 18 wherein said step of enhancing includes the steps of:

comparing said calculated value to predetermined limitations associated with physical limitations of an aircraft; and,

generating a fault signal when said calculated value exceeds said predetermined limitations.